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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,473	06/14/2001	Niels Knudsen	5150-47800	8104

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EXAMINER	
HA, DAC V	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,473	KNUDSEN, NIELS	
	Examiner	Art Unit	
	Dac V. Ha	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Response filed on 12/28/04.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Embree (US 6,104,222) in view of Adams (US 5,638,010).

Regarding claim 1, Embree discloses the claimed subject matter including "a preconditioner, wherein the preconditioner receives an input clock signal, wherein the preconditioner receives a master clock signal, wherein the preconditioner outputs a modified clock signal that is synchronized to the master clock signal" (Fig. 2, combination of elements 110, 120, 125, 130, 140; col. 3, lines 9-57), and

"a" "phase locked loop coupled to receive the modified clock signal output from the preconditioner, wherein the" "phase locked loop also receives the master clock signal, wherein the" "phase locked loop outputs an output clock signal, wherein the output clock signal is a version of the input clock signal synchronized to the master clock signal" (Fig. 2, element 150; col. 3, line 57 to col. 4, line 25); further Embree also implies the claimed subject matter "wherein the" "phase locked loop does not introduce phase noise to the synchronized version of the input clock signal" in col. 1, lines 58-65

in that, the introduction of element 150 into the system disclosed by Embree would overcome the noise condition in the prior art.

Embree differs from the claimed invention in that Embree does not diclose that the phase locked loop (PLL) is a "digital phase locked loop" (DPLL). Embree, however, suggests that any suitable PLL in the PLL technology could be utilized (col. 3, liens 3-8). In the same field of endeavor, Adams discloses the utilization of DPLL (Fig. 3). Since DPLL provides more accurate and higher speed, it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the PLL in Embree with a DPLL, as suitable, i.e., as the one in Adams, to improve overall operation of the system.

Regarding claim 2, Embree further disclose the claimed subject matter "wherein the preconditioner operates to noise shape phase noise of the synchronization to higher frequencies in col. 1, lines 16-34; and "wherein the distal phase locked loop operates to remove the phase noise at the higher frequencies" in col. 1, lines 58-65 in that, the introduction of element 150 into the system disclosed by Embree would overcome the noise condition in the prior art.

Regarding claim 3, Embree further disclose the claimed subject matter "wherein the preconditioner has a higher bandwidth than the digital PLL" in col. 5, lines 17-18, 26-27.

Regarding claim 4, Embree further disclose the claimed subject matter "wherein the preconditioner includes a loop having a loop gain, wherein the loop gain operates to attenuate phase noise introduced internal to the preconditioner" in col. 3, lines 31-32.

Regarding claim 5, as indicated earlier, it would be advantage to implement the PLL with a DPLL. Therefore, "preconditioner" of Embree constituted by combination of elements 110, 120, 125, 130, 140, would have been implemented with a DPLL (i.e., as that in Adams). With such combining in mind, Embree and Adams further discloses the claimed subject matter "a phase detector including a first input which receives the input clock signal and a second input, wherein the phase detector includes an output" (Embree, Fig. 2, element 120); "a loop filter having an input coupled to the output of the phase detector and including an output" (Embree, Fig. 2, element 125); "a voltage controlled oscillator (VCO) having an input coupled to the output of the loop filter and including an output" (Embree, Fig. 2, element 130"; "a latch having an input coupled to the output of the VCO, an input which receives the master clock signal, and including an output which generates the modified clock signal, wherein the latch synchronizes the modified clock signal to the master clock signal, wherein the output of the latch is coupled to the second input of the phase detector to provide the modified clock signal to the phase detector" (Embree, Fig. 2, element 140 and Adams, Fig. 3, elements 70, 85, 87, 88).

Response to Arguments

4. Applicant's arguments filed on 2/28/04 have been fully considered but they are not persuasive.

In the REMARKS, pages 4-5, applicant has argued "Applicant respectfully submits that Embree and Adams, whether alone or combined, fail to teach or suggest, "the preconditioner receives a master clock signal, wherein the preconditioner outputs a modified clock signal that is synchronized to the master clock signal" and "the digital phase locked loop also receives the master clock signal, wherein the digital phase locked loop outputs an

output clock signal, wherein the output clock signal is a version of the input clock signal synchronized to the master clock signal" as recited in independent claim 1. Embree fails to teach or suggest that the combination of elements 110, 120, 125, 130 and 140 receive "a master clock signal" as recited in claim 1 and that the PLL circuit 150 "also receives a master clock signal" as recited in claim 1. Embree further fails to teach or suggest that the output of VCO 130 (or the output element 140) and the output of PLL circuit 150 both are "synchronized to the master clock signal" as recited in claim 1. Additionally, Adams fails to teach or suggest "a preconditioner" as recited in claim 1, and Adams further fails to teach or suggest that the output of "a preconditioner" and the output of the DPLL circuit 45 both are "synchronized to a master clock signal" as recited in claim 1. Furthermore, Embree and Adams, whether alone or combined, fail to teach or suggest, "the digital phase locked loop does not introduce phase noise to the synchronized version of the input clock signal" as recited in independent claim 1. The Examiner contends that this feature is implied in Column 1 Lines 58-65 of Embree. The Applicant respectfully disagrees with the Examiner's assertion. Embree teaches, "However, such an approach requires a substantially lengthy period for the PLL system 10 to lock onto the input clock signal, because the input clock signal operates at a low frequency, typically 24 Hz. In addition, the PLL system 10 is susceptible to noise conditions such as power supply fluctuations, etc. To avoid the slow response time and instability of such a PLL system, a higher input clock frequency is used." (Embree, Column 1, Lines 58-65). The Applicant notes that the referenced section of the Embree patent highlights the shortcomings of the prior art by pointing out that the PLL system 10 is susceptible to noise conditions. Even it for the sake of argument, one assumes that Embree and Adams teach a mechanism that reduces the noise conditions associated with a system, Embree and Adams, whether alone or combined, fail to teach or suggest "the digital phase locked loop does not introduce phase noise to the synchronized version of the input clock signal" as recited in claim 1." It is, however, noted that in Embree, the reset signal (Figure 2), which synchronizes all the circuit component in system 10, teaches "the master clock", which is received by both "precoditioner" and the phase locked loop. Despite Embree implies the claimed subject matter "wherein the" "phase locked loop does not introduce phase noise to the synchronized version of the input clock signal" in col. 1, lines 58-65 in that, the introduction of element 150 into the system disclosed by Embree would overcome the noise condition in the prior art, such condition would have not been understood as not

absolute. Further, the examiner does not perceive how the claimed "digital phase locked loop does not introduce phase noise to the synchronized version of the input clock" given the fact that the phase locked loop, as well as any other electronic circuit, has inherent noise.

On pages 5-6, applicant has argued "Also, claim 2 recites, in part, "the preconditioner operates to noise shape phase noise of the synchronization to higher frequencies; wherein the digital phase locked loop operates to remove the phase noise at the hiqher frequencies". The Examiner contends that this feature is taught in Column 1 Lines 58-65 of Embree. The Applicant notes that the referenced section (Column 1, Lines 58-65) of the Embree patent highlights the shortcomings of the prior art by pointing out that the PLL system 10 is susceptible to noise conditions. The Applicant respectfully submits that Embree and Adams, whether alone or combined, fail to teach or suggest "the digital phase locked loop operates to remove the phase noise at the higher frequencies" as recited in claim 2. In accordance, claim 2 is believed to patentably distinguish over Embree and Adams, whether alone or combined." It is, however, noted that the system in Embree operates at higher frequency and also overcomes the noise drawback in the previous art (col. 1, lines 58-65).

With regard to last paragraph of the REMARKS, it is believed the combination of Embree and Adams does read on those claimed subject matter as indicated in the last office action.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dac V. Ha whose telephone number is 571-272-3040. The examiner can normally be reached on 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dac V. Ha
Primary Examiner
Art Unit 2634

05/16/05